Please add the following new claims:

40. (New) A method as recited in claim 8, wherein the obfuscation circuitry substantially increases the area of the electronic design or reduces the speed of a critical path of the electronic design.

41. (New) An apparatus as recited in claim 20, wherein the obfuscation circuitry substantially increases the area of the electronic design or reduces the speed of a critical path of the electronic design.

42. (New) A computer program product as recited in claim 32, wherein the obfuscation circuitry substantially increases the area of the electronic design or reduces the speed of a critical path of the electronic design.

43. (New) A method as recited in claim 37, wherein said entangler and scrambler circuitry substantially increases the area of said functional logic block and reduces the speed of a critical path of said functional logic block.

44. (New) A method as recited in claim 38, wherein said obfuscation circuitry and said additional flip-flops substantially increase the area of the electronic design.

45. (New) An intellectual property core as recited in claim 39, wherein said obfuscation circuitry substantially increases the area of said intellectual property core or reduces the speed of a critical path of said intellectual property core.

46. (New) A method as recited in claim 1 wherein said simulation model is cycle accurate and bit accurate.

47. (New) An apparatus as recited in claim 13 wherein said simulation model is cycle accurate and bit accurate.

48. (New) A computer program product as recited in claim 25 wherein said simulation model is cycle accurate and bit accurate.

49. (New) A method as recited in claim 37 further comprising:

producing a simulation model using said optimized intellectual property core, wherein said simulation model is cycle accurate and bit accurate.

50. (New) A method as recited in claim 38 further comprising:

producing a simulation model using said optimized intellectual property core, wherein said simulation model is cycle accurate and bit accurate.

51. (New) An intellectual property core as recited in claim 39 wherein said simulation model is cycle accurate and bit accurate.

52. (New) A method as recited in claim 3 wherein said functional logic block is an intellectual property core.

53. (New) An apparatus as recited in claim 15 wherein said functional logic block is an intellectual property core.

54. (New) A computer program product as recited in claim 27 wherein said functional logic block is an intellectual property core.

55. (New) A method as recited in claim 1, wherein the non-obfuscated version of the electronic design is provided in a partially compiled format, and wherein said creating a simulation model includes

using a translation utility to convert said obfuscated version of said electronic design into said simulation model having a standard format usable by a variety of simulators.

56. (New) An apparatus as recited in claim 13, wherein the non-obfuscated version of the electronic design is provided in a partially compiled format, said apparatus further comprising:

a model writer module that converts said obfuscated version of said electronic design into said simulation model having a standard format usable by a variety of simulators.

57. (New) A computer program product as recited in claim 25, wherein the non-obfuscated version of the electronic design is provided in a partially compiled format, and wherein said creating a simulation model includes

using a translation utility to convert said obfuscated version of said electronic design into said simulation model having a standard format usable by a variety of simulators.